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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/786,787	05/10/2001	Martin A. Cotton	2654-005US	6559

7590 10/23/2002

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EXAMINER	
DINH, TUAN T	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/786,787	COTTON, MARTIN A.
	Examiner	Art Unit
	Tuan T Dinh	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *02 April 2002* is: a)☐ approved b)☒ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "through hole in figure 13 has a convoluted shaped cross section" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 1-28 are rejected under 35 U.S.C. 102(b) as being anticipated by DiStefano et al (U. S. Patent 5,590,460).

As to claim 1, DiStefano a wiring connection structure for printed circuit board (95-figure 8, column 13, line 42) for interconnecting wiring circuit traces (36, 38) on a plurality of circuit trace layers (30, 36, 38, 64, 66-see figures 1-4) applied on a plurality of printed circuit board layers and electrically isolated there between by the printed

circuit board layers and having a printed circuit board multi-layer structure, characterized by:

a through hole (60-figure 4) with a **convoluted shaped cross section** having an interior wall (54, 58) that vertically extends through and intersects and exposes a plurality of wire circuit traces (26, 38) and having a plating of conductive material (76-figures 4 and 9) applied to the interior wall (54, 58) electrically connecting a plurality of wire exposed circuit traces on a plurality of circuit layers.

As to claims 2, 21-23, DiStefano discloses an EMI shielding structure as shown in figures 1-25 for a printed circuit board (95) for shielding wiring circuit traces (36, 38) on a plurality of circuit trace layers (see figures 1-4) applied on a plurality of printed circuit board layers and electrically isolated there between by the printed circuit board layers and having a printed circuit board multi layer structure, characterized by:

a trench (via 60) having a rim (55, column 11, line 26) about an opening of the trench at a top printed circuit board layer (see figures 1-9) and said trench (60) extending through a plurality of printed circuit board layers (95) to a grounding plane (200-figures 10-16, column 15, lines 8-9) exposing said grounding plane and said trench having an interior wall (54-figure 2) with a conductive plating material (76) applied over said wall (54) and said trench having a length greater than two times a breadth of said trench and said wall vertically extends around the perimeter of the printed circuit board and said plating electrically connects to said exposed ground plane and wraps over and laterally extends from said rim forming a lip.

As to claims 3-4, 8, 13, and 16, DiStefano discloses a wiring connection structure and a method as shown in figures 1-25 for a printed circuit board (95) for interconnecting a plurality of wiring traces (36, 38) applied on a plurality of printed circuit board layers (64, 66) and electrically isolated by printed circuit board layers and having a printed circuit board first layer with a main surface, characterized by:

a first wire trace (36) applied to said main surface (32) having a first terminal landing pad (100a) with a first through hole (88 of a contact 80) there through, said first through-hole having a convoluted shaped cross section with a continuous perimeter (see figures 5, 8-9);

a printed circuit board first insulation layer (64) formed over said first wire trace (36) having a second through hole (a hole between a wall 62) of identical cross sectional geometry to and vertically aligned with the first through hole (88) and extending to the first terminal landing pad (100a) exposing a portion of said first landing pad; and

a second wire trace (38) applied to the printed circuit board first insulation layer having a second terminal landing pad (100b) with a third through hole (88 of a contact 82) having identical geometry to and vertically aligned with the first and second through holes,

wherein said first, second and third through holes (formed as a through hole 60) are adjoining and are plated there through with an electrically conductive material forming a plated through hole with a convoluted cross section that vertically intersects the first and second terminal pads and electrically connects the first wire trace and the

second wire trace by a connection between the first and second wire trace terminal landing pads and the plated through hole.

As to claims 5-7, DiStefano discloses the structure as shown in figures 15, 17, 23, and 25 wherein the continuous curved cross section is U-shaped, L-shaped, or + shaped.

As to claim 9-12, DiStefano discloses a reference plane structure as shown in figures 1-25 for fixing a potential reference for a plurality of circuit trace layers (interposer 95) that are electrically isolated there between by the printed circuit board layers and having a printed circuit board first layer, characterized by:

a first wire trace circuit layer (36) applied to said main surface (32);

a first printed circuit board insulating layer (64) formed over said first wire trace circuit layer;

a first reference plane (100a) applied over the first printed circuit board insulating layer;

a trench (60) having an interior wall (54) and extending about a perimeter encompassing the first wire trace circuit layer and extending through the printed circuit board first layer, extending through and exposing the first wire trace circuit layer; extending through the first insulation layer and extending to the reference plane exposing the reference plane; and

a conducting plating layer on the interior wall (76) electrically connecting the first wire traces layer to the ground plane (200-figures 10-16); wherein the perimeter encompasses a portion of the first trace circuit layer (14).

As to claims 14-15, DiStefano discloses the structure as shown in figures 1-25 wherein the major diameter is at least about twice or three times that of the minor diameter (see figure 5).

As to claim 27, DiStefano discloses the structure as shown in figures 1-25 wherein said convoluted shaped cross section is square.

As to claims 17-19 and 28, since the method of manufacturing the device is merely a list of steps of forming, these steps must be performed in order to obtain the device (see rejection of claims 3-4, 8, and 13-16 above). Therefore, the method of manufacturing would be inherent to the shown structure of the device.

As to claim 20, since the method of manufacturing the device is merely a list of steps of forming, these steps must be performed in order to obtain the device (see rejection of claims 2, 9-12 above). Therefore, the method of manufacturing would be inherent to the shown structure of the device.

Allowable Subject Matter

1. Claim24 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. Claims 25-26 are allowed.

3. The following is an examiner's statement of reasons for allowance:

Neither the references cited nor the cited references do not teach or suggest the EMI shielding structure comprising an EMC sensitive track extending through a partial outer shield defined by a trench interior wall, a plating lip, and grounding plane.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

4. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan T Dinh whose telephone number is 703-306-5856. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-305-1341 for regular communications and 703-305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TD
October 17, 2002.

Albert W. Paladini 10-15-02
ALBERT W. PALADINI
PRIMARY EXAMINER